

REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-6 remain pending in the application. Claim 2 is amended by the present amendment. No new matter is presented.

In the Office Action, Claims 1-2 were rejected under 35 U.S.C. § 102(b) as anticipated by Kutaragi et al. (U.S. Patent No. 5,111,530, hereinafter "Kutaragi"); and Claims 3-6 were rejected under 35 U.S.C. § 103(a) as unpatentable over Kutaragi in view of Davis et al. (U.S. Patent No. 4,991,169, hereinafter "Davis").

Independent Claims 1-2 stand rejected under 35 U.S.C. § 102(b) as anticipated by Kutaragi. Applicant respectfully traverses these rejections.

Independent Claim 1 recites, in part, a data processor including a CPU, a DSP, and an external memory, in which

a data word length accessed by the DSP at the external memory is variable, and . . .

when the data word length is selected so that the DSP accesses the external memory using a maximum number of the bus cycles, when the determination unit determines that the DSP is accessing the external memory, access from the CPU to the external memory is placed in a wait state by the control unit

Applicant respectfully submits that Kutaragi does not disclose or suggest these features.

Kutaragi concerns an apparatus in which displacement of access periods can be adjusted by control of switches by a time-division circuit.¹ The Office Action asserts, at page 11, lines 1-4, that the number of cycles during which the Kutaragi DSP has access to the memory can be adjusted, thus disclosing that the length of the data word accessed can be changed. The Office Action further asserts, at page 4, lines 10-14, that the Kutaragi time-division control circuit can adjust the memory bus to be accessed by the DSP only, such that

¹ Col. 16, l. 30-32.

the CPU is not allowed to access the memory, thereby placing the CPU in a wait state. That is, the Office Action appears to assert that it is inherent to the Kutaragi apparatus that the length of the data word can be changed and that the CPU can be placed in a wait state.

Assuming *arguendo* that it is inherent that the length of the Kutaragi data word can be changed and that the Kutaragi CPU can be placed in a wait state, Applicant respectfully submits that it is *not* inherent that when the data word length is selected so that the DSP accesses the external memory using the maximum number of bus cycles in a unit of one data access, access from the CPU to the external memory is placed in a wait state, as recited in independent Claim 1. The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic.² In this regard, it is well established that inherency requires the certainty that something will happen, not merely a possibility or even a probability that something may occur.³ In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art.⁴

Applicant submits that changing the Kutaragi data word length does not require that the Kutaragi CPU be placed in a wait state. For example, the Kutaragi DSP might read the data word length over *two* units of data access. In such a case, the Kutaragi DSP might access the external memory using less than a maximum number of bus cycles in a unit of one data access. Meanwhile, the Kutaragi CPU might access the external memory by utilizing a free bus cycle. Accordingly, placing the Kutaragi CPU in the wait state will not necessarily happen. Thus, it is submitted that it is not inherent to Kutaragi that when the data word length is selected so that the DSP accesses the external memory using the maximum number

² In re Rijckaert, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); M.P.E.P. § 2112 (IV).

³ See In re Robertson, 49 USPQ2d 1949, 1951 (Fed. Cir. 1999).

⁴ Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990); M.P.E.P. § 2112 (IV).

of bus cycles in a unit of one data access, access from the CPU to the external memory is placed in a wait state, as recited in independent Claim 1.

Applicant additionally submits that independent Claim 2 patentably distinguishes over Kutaragi for the same reasons as discussed above with regard to Claim 1 and for the more detailed features presented in independent Claim 2.

Independent Claims 3 and 5 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Kutaragi in view of Davis. Applicant respectfully traverses these rejections.

Independent Claim 3 recites, in part, a data processor, including “an access determination unit configured to determine, when each of the DSPs issues a read command or a write command at a same time, which one of the DSPs is allowed to access the memory.” Applicant respectfully submits that Kutaragi and Davis fail to disclose or suggest these features.

The Office Action does not rely on Kutaragi for disclosing or suggesting the claimed access determination unit. The Office Action relies on Davis to remedy this deficiency in Kutaragi.

Davis concerns a DSP system in which DSP 20 and DSP 21 are mutually exclusive, as the Office Action concedes at page 11, lines 8-9. However, the Office Action asserts, at page 11, lines 9-11, that the Davis multiplexer is configured to determine which one of the DSPs is allowed to access the memory based on the select input of the multiplexer. That is, the Office Action appears to assert that it is inherent that, because the Davis multiplexer determines which one of the DSPs is allowed to access the memory, the Davis multiplexer must make such a determination when each of the DSPs issues a read command or a write command at a same time.

However, Applicant respectfully submits that the Davis multiplexer does not necessarily determine, when each of the DSPs issues a read command or a write command at

a same time, which one of the DSPs is allowed to access the memory. Indeed, the Office Action concedes that it is possible that the Davis DSPs never issue a read command or a write command at the same time.⁵ Accordingly, the Office has acknowledged that it is not certain that the Davis multiplexer makes a determination when each of the DSPs issues a read command or a write command at the same time. Therefore, it is submitted that Davis does not inherently disclose or suggest an access determination unit configured to determine, *when each of the DSPs issues a read command or a write command at a same time*, which one of the DSPs is allowed to access the memory, as recited in Claim 3.

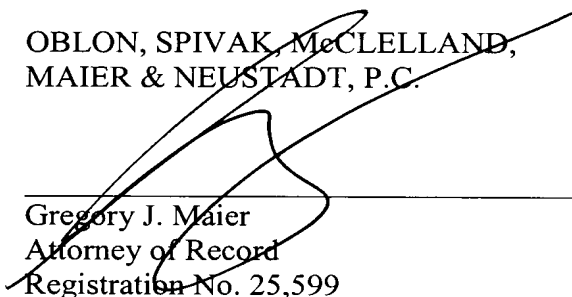
Therefore, Applicant submits that independent Claim 3 (and all associated dependent claims) patentably distinguish over Kutaragi and Davis. It is further submitted that independent Claim 5 patentably defines over Kutaragi and Davis for the same reasons as discussed above with regard to Claim 3 and for the more detailed features presented in independent Claim 5.

⁵ See Office Action at p. 11, l. 8-9.

Consequently, in view of the present amendment and in light of the foregoing comments, it is respectfully submitted that the invention defined by Claims 1-6 patentably distinguishes over the applied references. The present application is therefore believed to be in condition for formal allowance. An early and favorable reconsideration of the application is respectfully requested.

Respectfully submitted,

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